In the Claims:

1. (Currently Amended) A method of processing communication channels, comprising:

for each of a plurality of channels:

undertaking a given channel processing task for a given channel with one processor of a plurality of processors, said one processor optimized for said given channel processing task;

storing instance data for said given channel processing task in a memory which may be associated with any one of said plurality of processors such that said instance data is associated with said one processor;

when said given channel processing task for said given channel changes to a new channel processing task for which said one processor is not optimized,

moving processing of said given channel to a different one of said plurality of processors, said different one of said plurality of processors being optimized for said new channel processing task, and

changing association of said stored given channel instance data to an association with said different one of said plurality of processors ~~processor~~.

2. (Currently Amended) The method of claim 1 wherein said stored given channel instance data comprises a history buffer storing historical data samples for a signal on said given channel.

3. (Currently Amended) The method of claim 1 wherein said stored given channel instance data comprises a jitter buffer.

4. (Previously Presented) The method of claim 1 wherein said moving comprises consulting a table for a processor optimized to said new channel processing task.

5. (Original) The method of claim 1 wherein said memory is a multiplexed memory.

PAGE 3/11 * RCVD AT 4/21/2005 1:39:15 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/5 * DNIS:8729306 * CSID:919 654 4521 * DURATION (mm-ss):03-32

6. (Previously Presented) The method of claim 1 further comprising, wherein said one processor is optimized for said new channel processing task, undertaking said new channel processing task for said given channel at said one processor.

7. (Original) The method of claim 6 further comprising keeping a table with an identification of available ones of said plurality of processors and an identification of processing tasks handled by said available ones of said plurality of processors.

8. (Currently Amended) The method of claim 5 wherein said changing association comprises overwriting a latch holding an address of said one processor with an address of said different one of said plurality of processors ~~processor~~.

9. (Currently Amended) A method of processing communication channels comprising:

at each of a plurality of processors:

undertaking a channel processing task using a multiplexed memory having a plurality of channel memory partitions, each of the plurality of channel memory partition for storing channel instance data for a given channel;

when said channel processing task changes to a new channel processing task:

referencing a table to identify a new task optimized processor of said plurality of processors optimized to said new channel processing task,

prompting said new task optimized processor to assume processing of said given channel, and

arranging for an associator to associate the channel instance data stored in one of said plurality of channel memory partitions and associated with said given channel with said new task optimized processor.

10. (Currently Amended) A multiprocessor system for processing communication channels, comprising:

a plurality of processors, each optimized ~~optimised~~ for at least one channel processing task and each having processor memory for storing information associating different channel processing tasks to different ones of said plurality of processors;

PAGE 4/11 * RCVD AT 4/21/2005 1:39:15 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/5 * DNIS:8729306 * CSID:919 654 4521 * DURATION (mm-ss):03-32

a multiplexed memory for storing channel processing instance data for each of said plurality of processors;

an associator for associating channel processing instance data for each channel with one of said plurality of processors;

each processor of said plurality of processors operable to, on a channel processing task for a channel currently being processed by said each processor changing to a new task,

arrange for said associator to associate instance data for said channel with a processor optimized to said new task.

11. (Previously Presented) The system of claim 10 further comprising a host for, on a channel processing task for a channel currently being processed by a given processor changing to a new task, sending to said given processor an indication of said processor optimized to said new task.

12. (Original) The system of claim 10 wherein said associator comprises a latch for channel instance data of a given channel, each said latch being latched to a given processor processing said given channel and arranged such that only said given processor may change said latch to latch to a new processor.

13. (Original) The system of claim 12 wherein said associator further comprises a multiplexer mapping memory read/write requests from said given processor to instance channel data for said given channel in said shared memory.

14. (Original) The system of claim 13 wherein each of said plurality of processors is a digital signal processor ("DSP").

PAGE 5/11 * RCVD AT 4/21/2005 1:39:15 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/5 * DNIS:8729306 * CSID:919 654 4521 * DURATION (mm-ss):03-32